Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 3. (Canceled).

4. (Currently Amended) A data processing device, comprising:

an array of data processing units, the data processing units being connected to at least one of a power supply line and a clock line; and

an enabling/disabling device adapted to at least one of: i) enable or disable power supply to a number of the data processing units, and ii) block full clock speed for the number of data processing units;

wherein the number is less than all of the data processing units; and

wherein the enabling/disabling device is configured to be data driven, such that the enabling/disabling device at least one of disables the power supply and blocks the full clock speed for one of the number of the data processing units responsive to one of (a) an unavailability to the one processing unit of data that is to be processed by the one processing unit and (b) an inability to accept the data that is to be processed by the one processing unit.

5. (Previously Presented) The data processing device according to claim 4, wherein the enabling/disabling device is adapted to provide a clock to a number of the data processing units which is equal to 0.

6. (Previously Presented) The data processing device according to claim 4, wherein the enabling/disabling device is adapted to be handshake-driven.

7. (Previously Presented) The data processing device according to claim 4, wherein each of the data processing units is a reconfigurable unit of a multi-dimensional array.

8. (Previously Presented) The data processing device according to claim 4, wherein the enabling/disabling device is adapted to selectively enable or disable the power supply to the number of data processing units.

9. (Previously Presented) The data processing device according to claim 4, wherein the enabling/disabling device is adapted to selectively block full clock speed for the number of data processing units.

10. (Previously Presented) The data processing device according to claim 4, wherein the enabling/disabling device is adapted to be data availability driven.

11. (Previously Presented) The data processing device according to claim 4, wherein the number of data processing units includes only a single one of the data processing units in the array.

12. (Currently Amended) A data processing device, comprising:

an array of data processing units, the data processing units being connected to at least one of a power supply line and a clock line; and

an enabling/disabling device adapted to, in response to an availability status of data [[for]] to be processed by at least one respective one of the data processing units, at least one of: i) selectively enable or disable power supply to the at least one respective one of the data processing units, and ii) selectively block full clock speed for the at least one respective one of the data processing units;

wherein the at least one respective one of the data processing units includes less than all of the data processing units in the array.

13. (Previously Presented) The data processing device according to claim 12, wherein the enabling/disabling device enables the power supply to the respective one of the data processing units only when data is available for the respective one of the data processing units.

14. (Previously Presented) The data processing device according to claim 12, wherein the enabling/disabling device is adapted to make a clock signal available to the respective one of the data processing units only when an operand is ready for the respective one of the data processing units.

15. (Previously Presented) The data processing device according to claim 12, wherein the enabling/disabling device is associated with only a single one of the data processing units.

16. (Previously Presented) The data processing device according to claim 12, wherein the at least one respective one of the data processing units includes only a single one of the data processing units in the array.

17. (Previously Presented) A data processing device, comprising:

an array of data processing units, the data processing units being connected to at least one of a power supply line and a clock line; and

an enabling/disabling device adapted to make a clock signal available to at least one respective one of the data processing units when an operand is ready for the at least one respective one of the data processing units; and

wherein the at least one respective one of the data processing units includes less than all of the data processing units in the array.

18. (Previously Presented) The data processing element according to claim 17, wherein the enabling/disabling device is associated with only a single one of the data processing units.

19. (Previously Presented) The data processing device according to claim 17, wherein the at least one respective one of the data processing units includes only a single one of the data processing units in the array.

20. (New) A reconfigurable device for data processing via a dynamical runtime reconfiguration method, comprising:

a plurality of processing array elements that are reconfigurable at a runtime by reconfiguration information;

a plurality of configurable data busses adapted to transmit data in a multi-dimensional way, at least some of the plurality of processing array elements configurable for connection to said busses to provide non-next-neighbor connections, wherein said at least some processing array elements include coarse grained units for arithmetic and logic operations, at least one of the coarse grained units including:

a stage for arithmetic operations, the stage including a multiplier stage and an adder stage;

at least one input and at least one output for data;

a first plurality of registers;

a return path; and

at least one multiplexer;

a program load unit; and

an interconnection selection unit adapted to selectively interconnect said at least one of the coarse grained units with others of the coarse grained units;

wherein:

a first subset of said first plurality of registers is provided for said at least one input and at least one output and allows for decoupling of said at least one input from said busses by storing of operand inputs;

said multiplier stage is connectable to: (a) at least two input registers of said first subset for receiving an input of two operands; and (b) said adder stage, said connections to (a) and (b) being such that a selection can be made between at least two of:

(i) adding two operand inputs;

(ii) adding an output of said multiplier stage and a further operand input;

(iii) the output of said multiplier stage and results of the at least one coarse grained unit; and

(iv) an operand input and an output of a result of the at least one coarse grained unit;

said return path is adapted to return a result of said at least one coarse grained unit from an output register of said first subset as an operand via said at least one multiplexer for selecting for further processing one of an external operand input and a result;

said at least one multiplexer is arranged between an input register of said first subset and said adder stage so as to allow said at least one coarse grained unit to selectively have direct access to its own results which are returned as operands for calculations in a serial manner;

said at least one adder stage is bypassable by allowing for an addition of a zero as one operand input;

said plurality of processing array elements are partially dynamically reconfigurable at run time in their function; and

the function and an interconnection of said plurality of processing array elements are programmed in units specifically accessible by a program load unit.

21. (New) The reconfigurable device of claim 20, wherein said plurality of processing array elements are partially dynamically reconfigurable at run time in their interconnection.

22. (New) The reconfigurable device of claim 21, wherein at least some registers of the reconfigurable device are shift registers that provide shift capabilities.

23. (New) The reconfigurable device of claim 22, wherein said plurality of processing array elements includes at least one array element having an arithmetic and logic unit, a bus access from a data processing in said arithmetic and logic unit being decoupled via registers so that said at least one array element is independently functional.

24. (New) The reconfigurable device of claim 23, further comprising:

a second plurality of registers which communicate with the at least one coarse grained unit for storing data relating to a configurable function of the at least one coarse grained unit and data relating to an interconnection of stages within the at least one coarse grained unit.

25. (New) The reconfigurable device of claim 24, wherein said program load unit is configured for:

accessing specific registers of said second plurality of registers for at least one of:

storing the data relating to the configurable function;

selectively transferring to said specific registers the data relating to the configurable function; and

selectively transferring to said specific registers the data relating to the configurable interconnection.

26. (New) The reconfigurable device of claim 25, wherein the data relating to the configurable function of and the interconnection of stages within the at least one coarse grained unit forms a configuration vector that is set through a function control interface and refers to a number of possible instructions, said possible instructions being such that, for any one of the number of possible instructions, a response of any one of the at least some of the plurality of processing array elements to said data that refers to the number of possible instructions is identical to a response of any other of the at least some of the plurality of processing array elements to said number of possible instructions, said responses remaining the same over time such that transmitted ones of the number of possible instructions statically correspond to a constant one of possible operations.

27. (New) The reconfigurable device of claim 20, wherein the units specifically accessible by the program load unit are registers.

28. (New) The reconfigurable device of claim 27, wherein the reconfigurable device is adapted for reconfiguring said plurality of processing array elements in their function and interconnection at run time such that data processing by at least some of said plurality of processing array elements is not inhibited while data relating to a configurable function of and an interconnection of stages within another of said plurality of processing array elements is transferred to ones of the specifically accessible registers.

29. (New) The reconfigurable device of claim 28, wherein a register decoupling from a bus of said other processing array elements when said another processing array element is reconfigured by the reconfiguration information at runtime allows the reconfiguration of said another processing element without an interfering effect on data transmitters and receivers in the at least some of said plurality of processing array elements, such that: said plurality of processing array elements are partially reconfigurable; and the at least some of said plurality of processing array elements are able to continue their data processing during the partial reconfiguration.